E-Smog detector PCB Design

EV6 - Hardware Implementation

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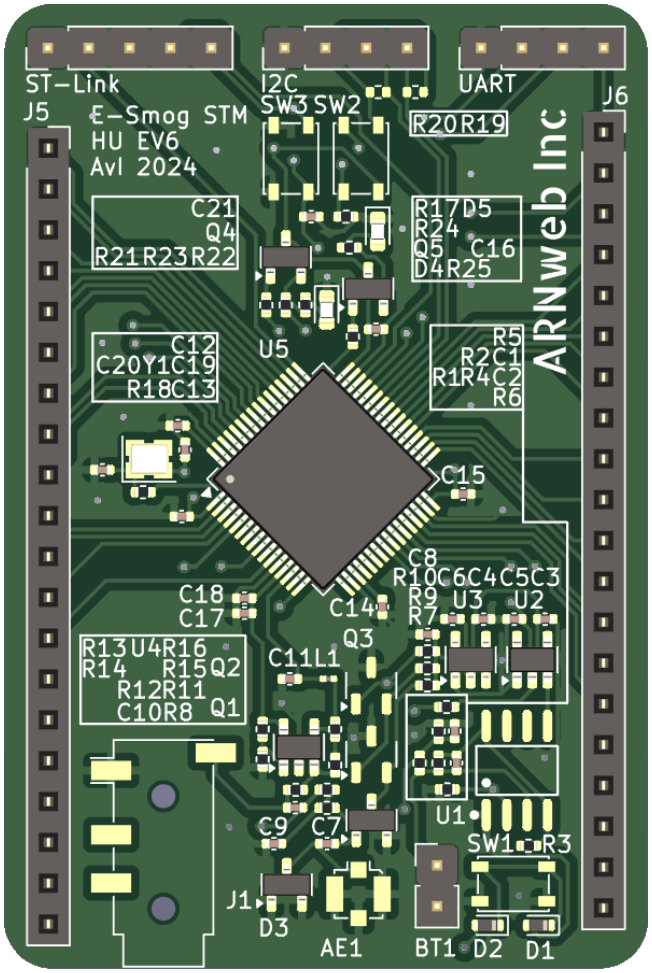


Abstract

This document will describe the design process of a noise detection circuit (E-Smog) and data logger using an STM32 Microcontroller

1 Introduction

Electronic Smog or E-Smog is electromagnetic radiation emitted by every electronic device. The radiation can interfere with sensors and microphones, in extreme cases, the radiation can be harmful for human beings and animals. The TAPIR E-Smog detector is a circuit featured in Elektor Magazine issue 585 to measure said electromagnetic radiation. [1]

Figure 1: Man holding commercial ESmog detector

Engineering Students of the University of Applied Sciences Utrecht have been tasked with designing a PCB for this circuit while extending the function of the circuit by including a STM32 microcontroller to log the amount of E-Smog detected.

2 Design choices

The complete circuit has been divided into several parts, each with its own function. The following sections will describe the design choices made for each distinct part of the circuit.

2.1 Power supply

The following parts can be found in the KiCad schematic sub-sheet 'power'.

2.1.1 Voltage regulators

The circuit requires two voltages; 1,5 volts for the amplifier circuit and 3,3 volts for the STM32. The input voltage will be roughly between 3.0 and 3.6 volts based on three NiMH rechargeable batteries in series.

The amplifier circuit is rated to work at 1,5 volts, however, 1,5 volt low dropout regulators are not common. 1,8 volts is a lot more common, therefore the circuit has been simulated with 1,8 volts instead. The simulation of the circuit has been performed in NI Multisim 14.2, the circuit in question will be included in the appendix.

The output voltage of the simulated circuit is offset slightly higher at 1.8 Volts compared to 1.5 Volts, as measured at C4 in Figure 3 the voltage offset is 669 millivolts instead of 639 millivolts. This is a difference of 30 millivolts, which is acceptable for the purpose of the circuit.

The increased current flow is also negligible, increasing from 1.04 milliamps to 1.37 milliamps.

2.1.2 Soft power-on circuit

To turn the device on, a soft power-on circuit has been implemented. The circuit is based on the design by A. Levido and consists of a set of P- and N-channel MOSFETs, a push button and two schottky diodes. [2] In the schematic, the IRF7319 package is used, which contains both the P- and N-channel MOSFETs.

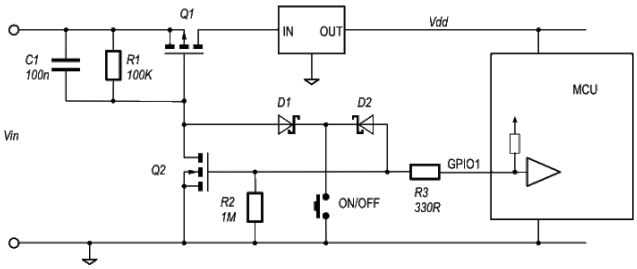


Figure 2: Soft power-on circuit by A. Levido

The P-Channel MOSFET is in between the battery and the LDO's, when the user presses the button the P-Channel closes and allows the circuit to power on, once the STM has booted, it closes the N-Channel that will keep the circuit on for the duration of the program. The push button is connected via two schottky diodes so it can double as a regular input button for the STM.

The logger was, as first, supposed to have an SD card to store logs to and a sudden power off could damage the file system of the SD card. The power button also pulls an IO pin on the STM32 low and this would be used to trigger a graceful power off sequence. The SD card has since been removed from the design but the soft power-on circuit has been kept.

2.1.3 Battery voltage feedback

The battery voltage is measured using a voltage divider and fed into the STM32 ADC. While this is a simple voltage divider. This is a very simple way to measure the battery voltage that has the disadvantage of constantly depleting the batteries, although very slowly. Using the current design, using two 1M resistors, the current flow is as follows:

$$
\begin{aligned}
R_{total} &= 2 && [M\Omega] \\
U &= 3.6 && [V] \\
I_{total} &= \frac{U}{R_{total}} \\
&= \frac{3.6}{2 \cdot 10^{6}} \\
&= 1.8 \cdot 10^{-3} && [mA]
\end{aligned}
$$

The self-discharge of the batteries is significantly higher than the current flow of the voltage divider, so the impact of the voltage divider is negligible.

2.2 E-Smog circuit

The following parts can be found in the KiCad schematic sub-sheet 'smog'.

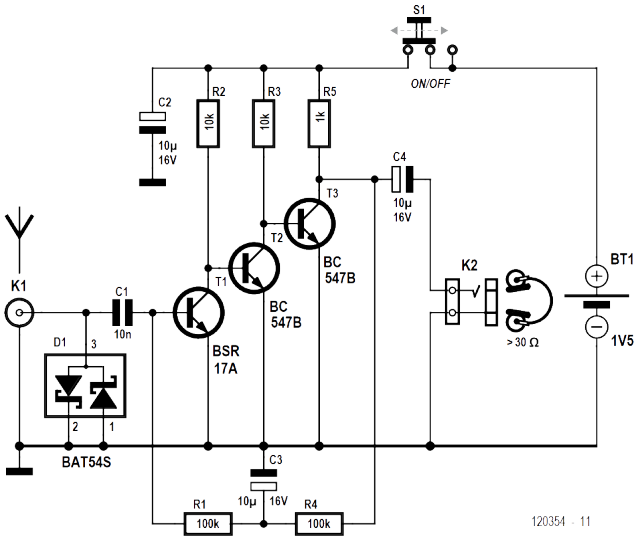


Figure 3: Original Circuit

2.2.1 Base circuit

The base receiving circuit is functionally identical to the one found in the original Elektor Magazine. The required transistors have been replaced with SMD equivalents.

The antenna uses a Hirose U.FL connector, this connector is a small SMD component, commonly used in customer radio equipment such as access points and routers; This connector has primarily been chosen for this reason as it allows salvaging a simple wire antenna from such a device. It also allows for a smaller footprint compared to the RCA connector used on the original design.

2.2.2 Amplifier

The amplifier circuit is required to bring the signal from the E-Smog circuit to a level that is measurable by the STM32 ADC. The amplifier is a simple inverting op-amp circuit with a gain of 3 and an offset of 1.5 volts to get it around the middle of the ADC range. The LM321 has been used as the op-amp, this is a low power op-amp that can run on a single supply voltage. It is also fast enough for the desired purpose. The resulting simulated output to the ADC is offset at 1.5 volts and has a signal V_{p-p} of 740 millivolts.

2.2.3 Anti-aliasing filter

For the ADC input, we want to attenuate the input signal above the Nyquist frequency to less than half LSB to prevent any aliasing.

The STM32L071 has a 12-bit ADC with a maximum sampling rate of 1.14Msps. The Nyquist frequency is half the sampling rate, so 570kHz. For a 12 bit ADC, this LSB value is as follows:

$$\begin{aligned} U_{ref} &= 3.3 && [V] \\ LSB &= \frac{U_{ref}}{2^{12}} \\ &= \frac{3.3}{4096} \\ &= 0.0008056641 && [V] \\ &= 0.806 && [mV] \\ \frac{1}{2}LSB &= 0.403 && [mV] \end{aligned}$$

The amplifier can output 3.3V, so the input signal should be attenuated by a factor of:

$$20 \cdot \log \frac{0.403e^{-3}}{3.3} = -78,26 \qquad [dB]$$

Since the circuits purpose is to measure E-Smog within the hearing range, the cutoff should ideally be near between 10 and 20 kHz. Attenuating the signal to a factor of -80dB at 570kHz would mean a cutoff frequency of 5,7 kHz using an LRC filter with a -40dB/decade slope, this is simply not acceptable.

Using the full 12-bits of the STM would reduce the amount of bandwidth and maximum measurable frequency, instead, the 10 bit mode of the ADC will be used. While this does limit resolution, the difference will be small since the effective resolution of the particular STM used is only 10.2 bits. [3] This makes the LSB and cutoff frequency:

$$\begin{aligned} U_{ref} &= 3.3 && [V] \\ LSB &= \frac{U_{ref}}{2^{10}} \\ &= \frac{3.3}{1024} \\ &= 0.003222656 && [V] \\ &= 3.223 && [mV] \\ \frac{1}{2}LSB &= 1.611 && [mV] \end{aligned}$$

$$20 \cdot \log \frac{1.611e^{-3}}{3.3} = -66.23 \qquad [dB]$$

$$\begin{aligned} f_{cutoff} &= 570000 \cdot 10^{-\frac{66.23}{40}} \\ &= 570000 \cdot 10^{-1.65575} \\ &= 12595.33 && [Hz] \end{aligned}$$

The required filter has been implemented using a LRC filter. The required parameters have been determined using the *RLC Low-Pass Filter Design Tool* by OKAWA Electric Design. [4] A capacitor of $6.8\mu F$ and a inductor with a value of $22\mu H$ and an internal resistance of 3.6Ω have been selected. The CWCI0603F-220KT package from Ceaiya has been selected as the inductor and resistor, a regular 0402 SMD capacitor completes the filter.

The resulting filter has been simulated and generates the following Bode plot:

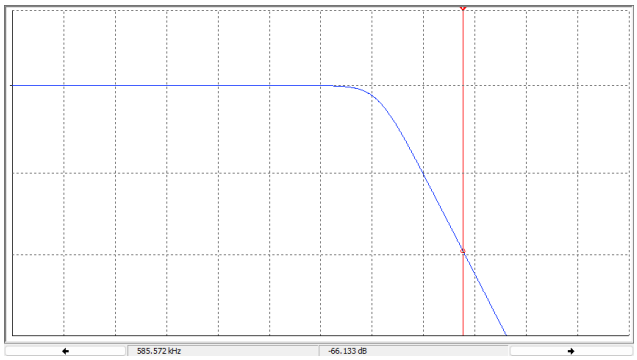


Figure 4: Bode plot filter

The bode plot shows the -66dB attenuation is roughly at the desired 570kHz and the cutoff frequency is at around 9kHz. This is not ideal but acceptable.

2.3 Microcontroller

The following parts can be found in the KiCad schematic sub-sheet 'stm'.

2.3.1 Choice of microcontroller

The assignment requires the use of a STM32L series microcontroller; This is the low power series of the STM32 line. The entire series is relatively easy to implement and most if not all design choices in the following section are based directly on the AN4467 Application note by STMicroelectronics [5]

The STM32L071RBT has been selected with the help of the STM32 MCU product selector. The STM32L071RBT is available in a small but workable LQFP64 package and can be powered by a single 3.3 Volt supply. It has plenty of GPIO pins and a 12-bit ADC. All STM32L series microcontrollers use the ARM Cortex-M0+ core, so the selection was mostly based on the availability of the part itself. The STM32L071RBT is available as a Basic part on JLCPCB.

2.3.2 Peripheral connections

The STM32 has the following peripheral connections:

- Programming and debugging header present, connected to SWD. The pinout of this header has been determined by the application note [5]
- I2C and UART are broken out to marked header pins
  - I2C has unpopulated pads for pull-up resistors if these are not provided by the slave device(s).
- NRST and BOOT0 are connected to buttons in accordance to the application note [5]
- All VCC pins have a decoupling capacitor nearby in accordance to the application note [5]
- An external crystal is used for the HSE, connection as described in the data sheet [3]
- Two LEDs are connected to GPIO pins via a MOSFET driver
  - The power LED is connected to the same pin used as the power button override as described in section 2.1.2, this allows the user to see when the STM has powered up.
- All other IO has been broken out to headers J5 and J6

3 Printed Circuit Board design

Similarly to the schematic, the PCB components have been placed in groups. Analog and digital switching components have been separated as much as possible. The PCB has been routed using the maze-method, X, Y-routing has been considered but ultimately not used. The resulting PCB would have been much more complex then necessary, since there are no high-speed signals that would benefit from X, Y-routing. Routing below the analog components has been kept to a minimum to prevent interference.

3.1 Routing IO

Breaking out all remaining MCU pins to the side of the PCB may not have been the greatest idea of all time and required some compromises. The STM32 microcontroller has been placed on a 45 degree angle to simplify the routing of all IO pins, however it still required long paths between the MCU and the headers. Additionally, the paths to the headers are placed quite close to each other which may cause interference, making the bus unusable for very high speed signals; This is not a problem for the intended use of the circuit.

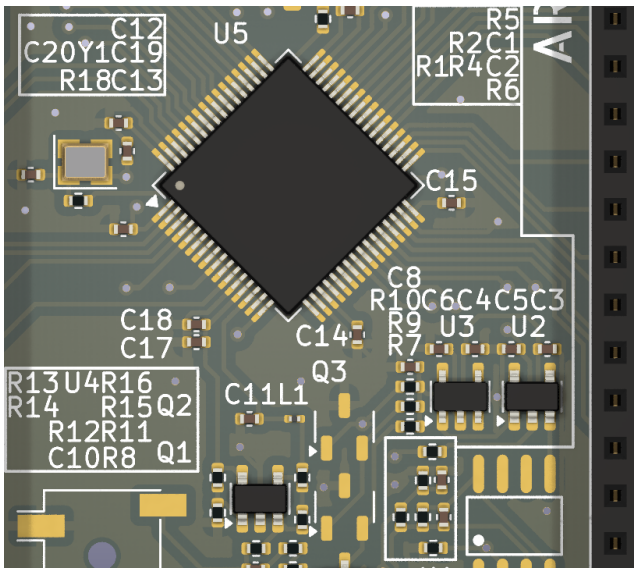


Figure 5: Reference blocks in the silkscreen

To route the IO, all other SMD parts have been packed closely together, which does not necessarily impact performance, but does make the PCB harder to assemble and required the use of reference blocks in the silkscreen to identify the components. An example of this can be seen in Figure 5, take for example R5. Placing the silkscreen next to a component, such can be seen at C18, would have been preferable.

3.2 DRC check

The PCB has been checked using the default rules for DRC in KiCAD in addition to design rules set by the manufacturer JLCPCB, the end product does not contain any DRC errors.

4 Peer reviewed corrections

The following corrections have been made based on the peer review checklists in the appendix. Tom Selier noted the following issues from his checklist:

- Ground planes were not well connected
- Decoupling capacitors did not have a fast path to ground
- PCB dimensions were not present
- Some components did not have proper thermal isolation from the ground plane
- Voltage rails do not use thicker traces

Most of these issues have been resolved, the ground planes have been enlarged where possible and more via's were used to connect them. Decoupling capacitors have been checked and the ground connection has been improved wherever possible. The PCB dimensions, although not strictly required, were added to the bottom silkscreen of the board. Lastly, some components have been moved in order to improve thermal isolation from the ground plane and other components.

An issue that was not fixed was the use of thicker traces for the voltage rails, this could not be fixed without redesigning significant portions of the design; Which could not be done given the time constraints of the assignment. However, to ensure the current design would not cause a house fire, the current specifications of the traces have been checked using the *PCB Trance Width Calculator* by DigiKey [6].

The current design uses three AAA batteries as a source of power, these batteries have a (very short) maximum current output of around 1 Ampere, this value is between 750 and 900 mA for NiMH cells. If the PCB is at JLCPCB, the top trace thickness would be $70\mu m$

Using these parameters in the calculator and assuming the worst case scenario of 1 A, the minimum trace width would be 0,065 mm. The current design uses a trace width of 0,25 mm, which is well in the safe zone.

5 Conclusion

Although there is room for improvement, the current design is functional and meets the requirements set by the assignment. The design has been checked using Multisim and the ERC and DRC checks in KiCad. The design has been peer-reviewed and the resulting corrections have been implemented. If the design were to be produced, the design is likely to work as intended.

References

[1] Elektor International Media BV, "Elektor magazine," vol. 585/586, July/August 2012.

[2] A. Levido, "Soft latching power circuits," *Circuit Cellar*, September 2021. [Online]. Available: https://circuitcellar.com/resources/quickbits/soft-latching-power-circuits/

[3] STMicroelectronics, "Stm32l071x8 stm32l071xb stm32l071xz," November 2019, datasheet - production data. [Online]. Available: https://www.st.com/resource/en/datasheet/stm32l071v8.pdf

[4] Okawa Electronic Design, "Rlc low-pass filter design tool," 2024. [Online]. Available: http://sim.okawa-denshi.jp/en/RLClowkeisan.htm

[5] STMicroelectronics, "Getting started with stm32l0xx hardware development," January 2015, application note AN4467. [Online]. Available: https://www.st.com/resource/en/application_note/an4467-getting-started-with-stm32l0xx-hardware-development-stmicroelectronics.pdf

[6] DigiKey, "Pcb trace width calculator," 2024. [Online]. Available: https://www.digikey.com/en/resources/conversion-calculators/conversion-calculator-pcb-trace-width

6 Appendix

6.1 Peer review checklists

6.1.1 Peer checklist (Dutch, Tom Selier)

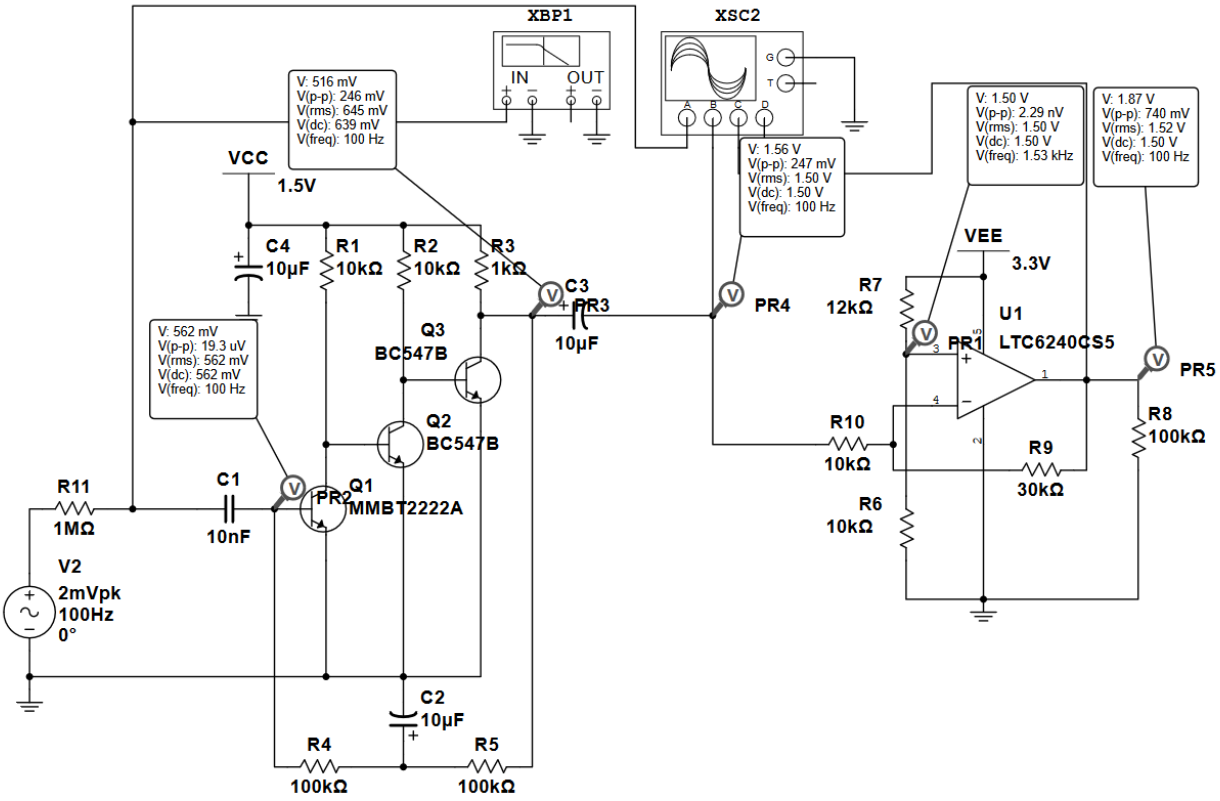
1. DRC van een PCB boer zijn geïmporteerd
2. DRC geeft geen bijzondere meldingen
3. Trace width presets zijn logisch en correct gebruikt
4. Geen losse kopervlakken
5. Grondvlakken zijn goed verbonden met elkaar
6. Ontkoppeling heeft een snel en logisch pad naar grond
7. Maatmarkeringen zijn aanwezig
8. Thermische scheiding is in acht genomen
9. Capillaire kracht is in acht genomen (tombstoning e.d.)
10. Alle componenten hebben een footprint en zijn aanwezig
11. Beschikbare ruimte is benut
12. Componenten zijn gegroepeerd op functie
13. Digitaal en analoog zijn zoveel mogelijk gescheiden
14. "Peelables" zijn z.v.m. voorkomen
15. Naam en functie staan op silkscreen

6.1.2 Own checklist

1. ERC and DRC checks have been performed
2. Component placement is logical when cross-referenced with the schematic
3. Analog and digital circuits are separated
4. The PCB has been filled with ground planes
5. All filled areas are well connected
6. Via's between filled ares are not on the very edge of the filled area
7. Components connected to the filled area are connected by more than one spoke
8. The PCB only has components on one side
9. Digital interface requirements have been met (e.g. I2C pullups)
10. Switches and buttons are usable when the PCB is assembled
11. Decoupling capacitors are placed near the power pins of the IC
12. Most of the MCU pins used or broken out to headers
13. Headers other than the GPIO have been marked with their purpose
14. Silkscreen references are either next to the component or in a collection
15. Silkscreen references are visible after PCB assembly
16. The silkscreen features the name of the designer

6.2 Multisim simulation

6.2.1 Analog circuit



Weerstand want een antenne heeft een flinke impedantie

Figure 6: Multisim simulation of the analog circuit

6.2.2 Filter circuit

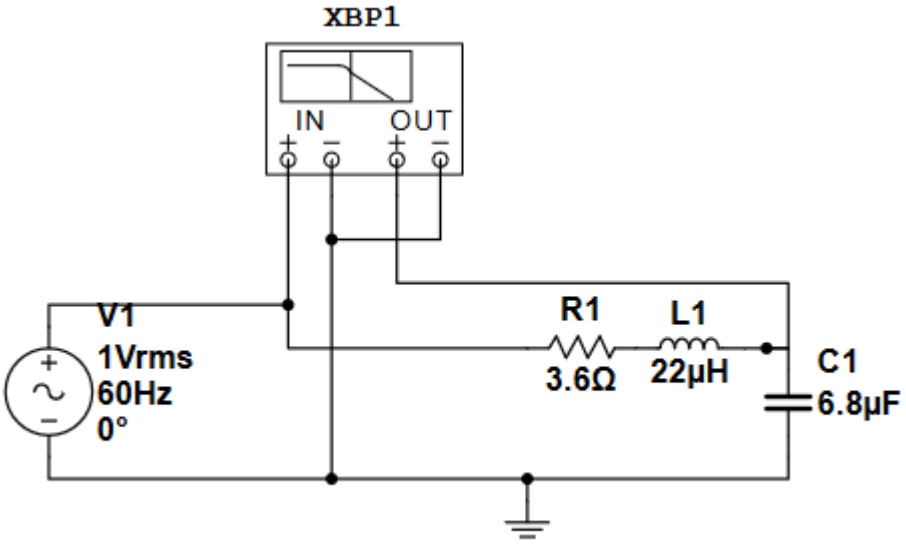
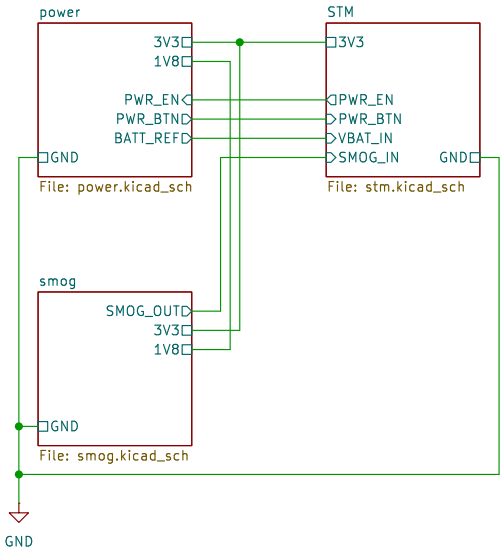


Figure 7: Multisim simulation of the filter circuit

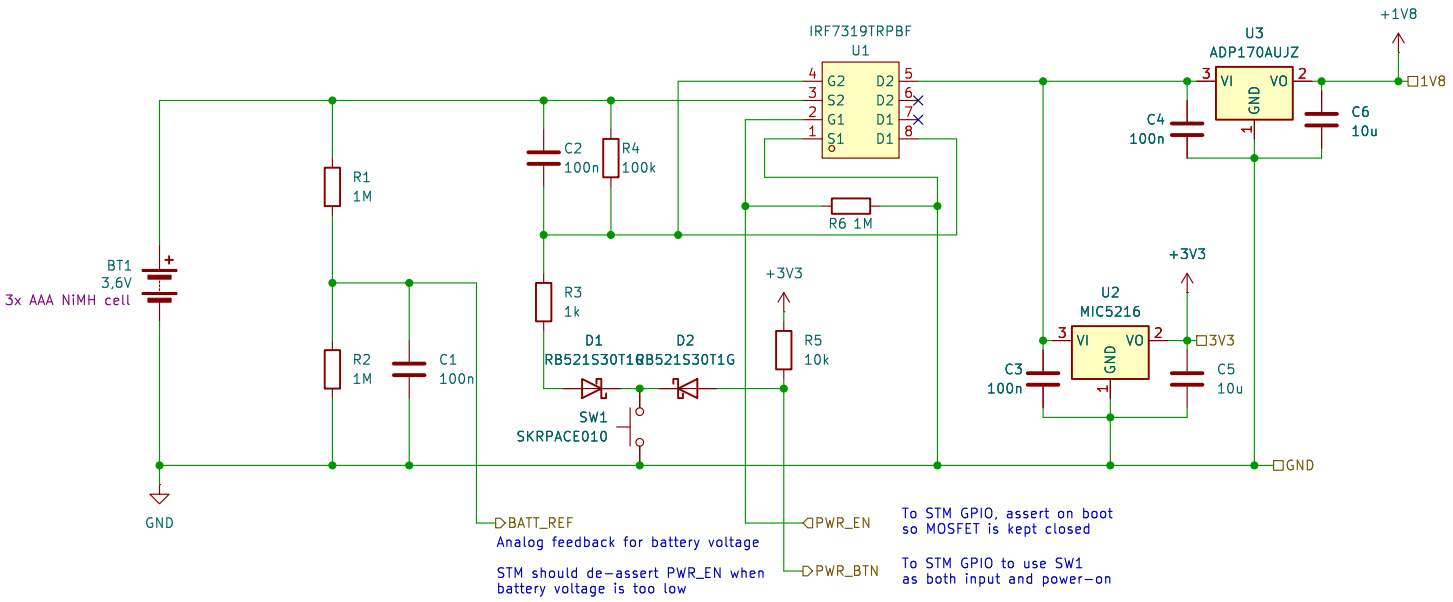
6.3 KiCad Export

The following exports will be appended to the document in the following order:

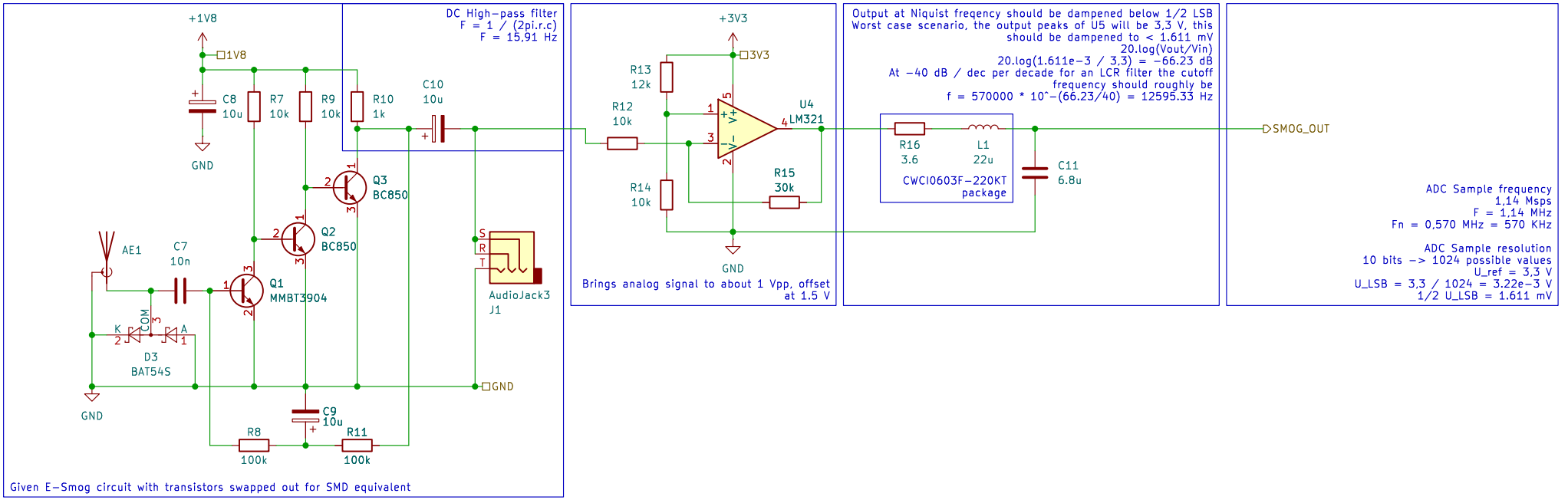
1. Schematic
    - Sub-sheet 'power'
    - Sub-sheet 'smog'
    - Sub-sheet 'stm'
2. PCB
    - Top layer
    - Bottom layer
    - Silkscreen top
    - Silkscreen bottom



Arne van Iterson		
1798423		
ARNweb Inc.		
Sheet: /		
File: e-smog.kicad_sch		
Title: E-Smog detector		
Size: A4	Date: 2024-03-15	**Rev: 0.2**
KiCad E.D.A. 8.0.0		Id: 1/4



Arne van Iterson		
1798423		
ARNweb Inc.		
Sheet: /power/		
File: power.kicad_sch		
Title: E-Smog detector Power		
Size: A4	Date: 2024-03-15	**Rev: 0.2**
KiCad E.D.A. 8.0.0		Id: 2/4



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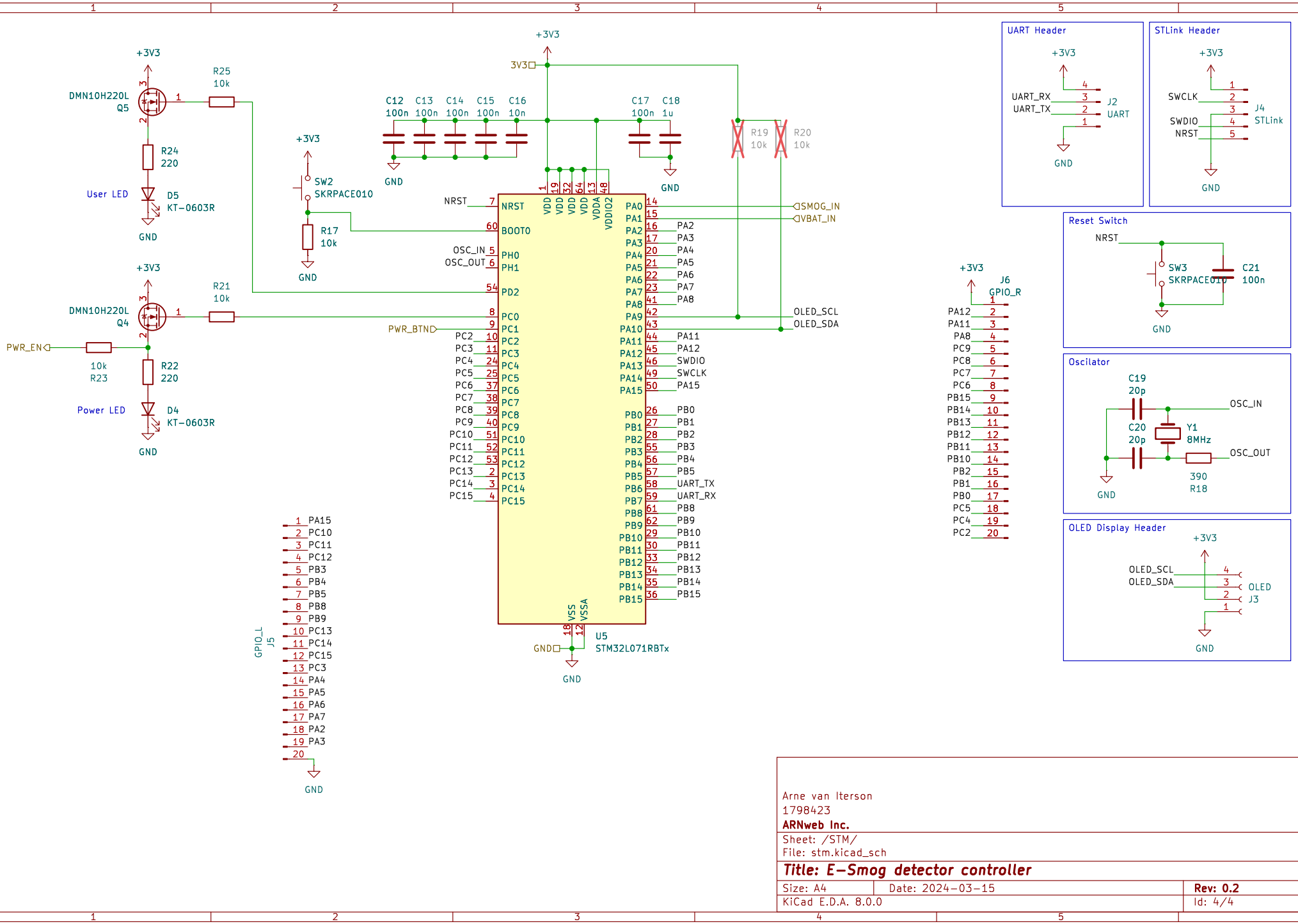
ARNweb Inc.

Sheet: /smog/
File: smog.kicad_sch

Title: E-Smog detector receiver

Size: A4	Date: 2024-03-15	**Rev: 0.2**
KiCad E.D.A. 8.0.0		Id: 3/4



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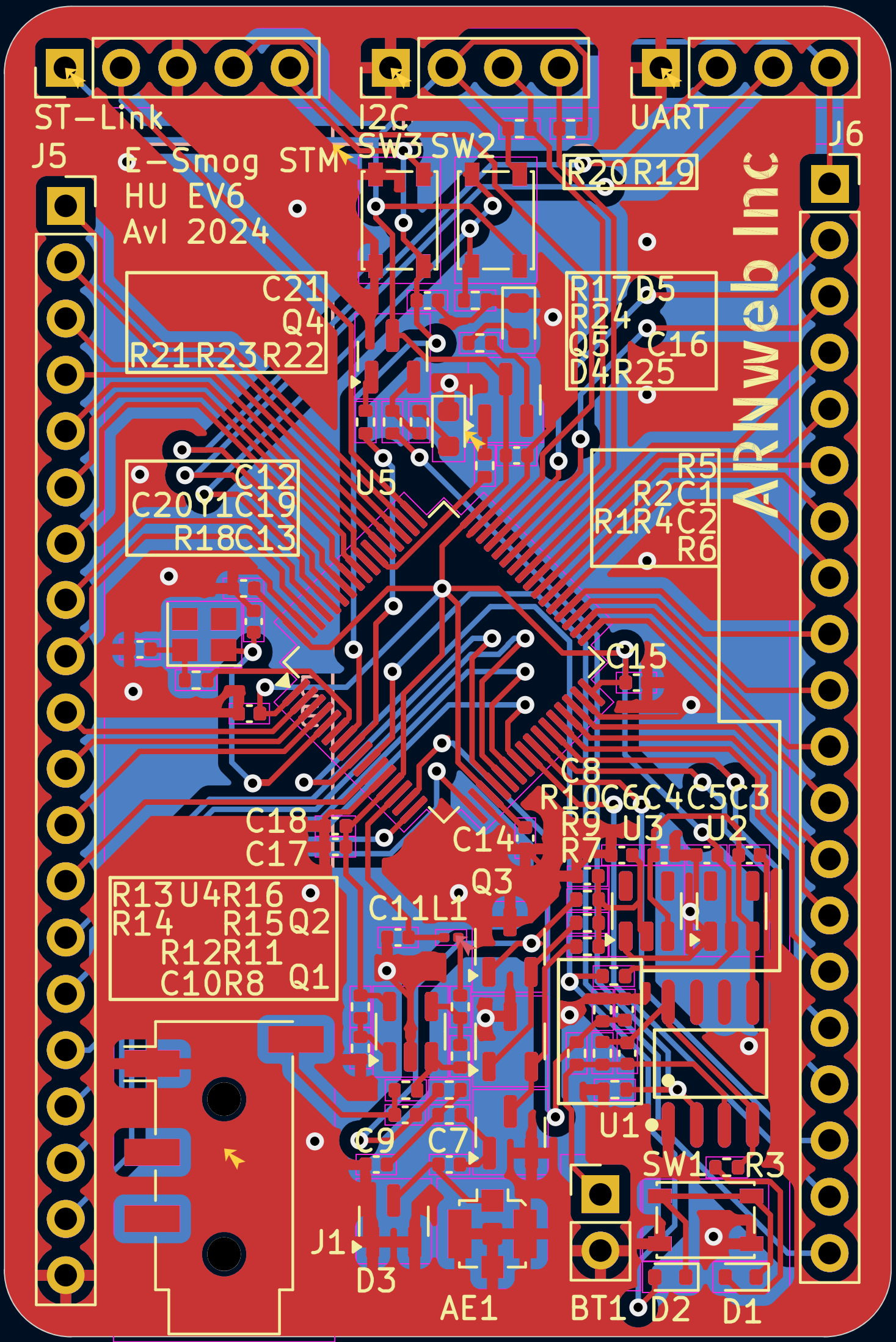
1798423
ARNweb Inc.

Sheet: /STM/
File: stm.kicad_sch

Title: E-Smog detector controller

Size: A4	Date: 2024-03-15	**Rev: 0.2**
KiCad E.D.A. 8.0.0		Id: 4/4


ST-Link
J5
I2C
UART
J6
E-Smog STM
HU EV6
Avl 2024
SW3
SW2
R20
R19
C21
Q4
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R22
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ARNweb Inc
C12
C20
Y1
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C6
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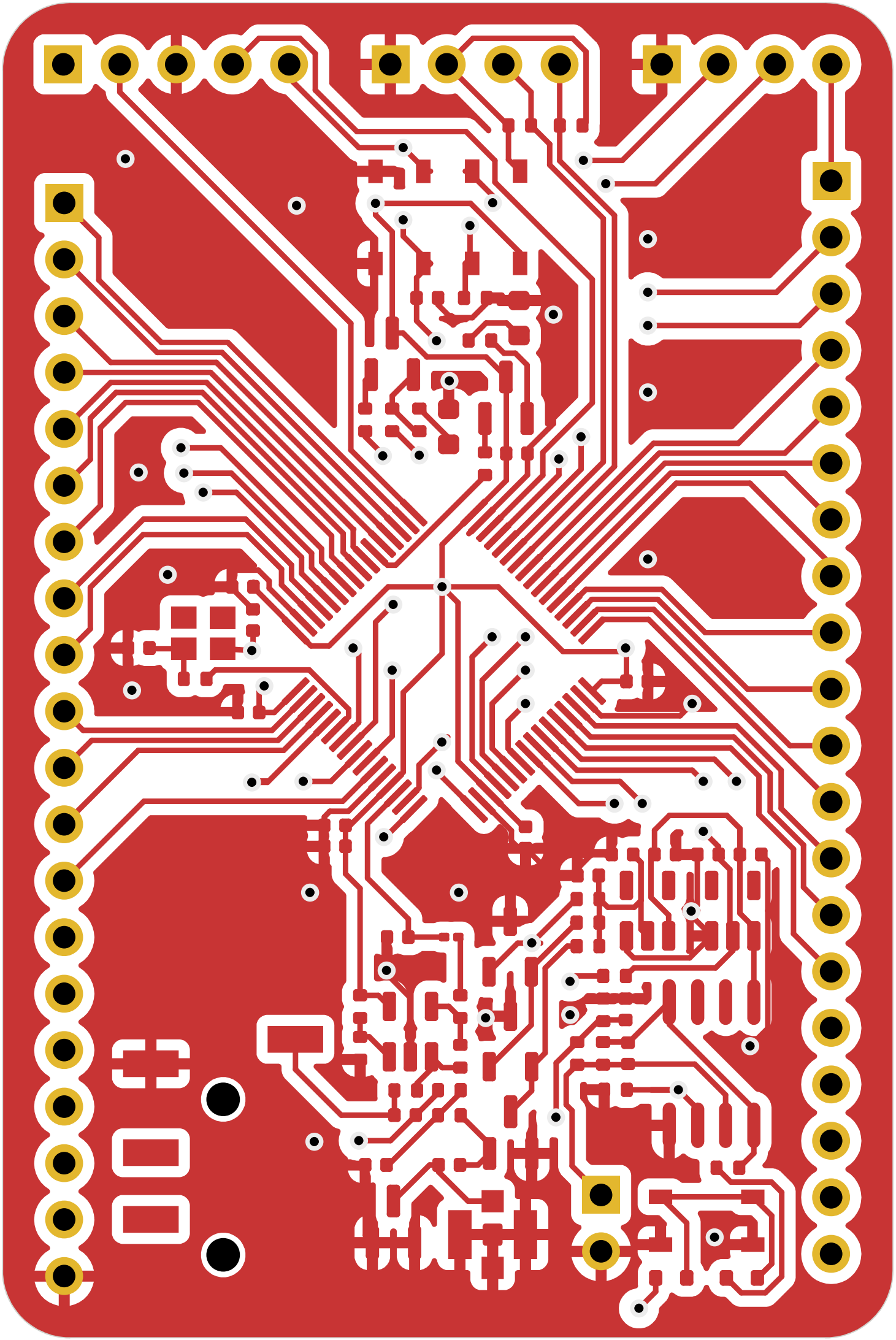
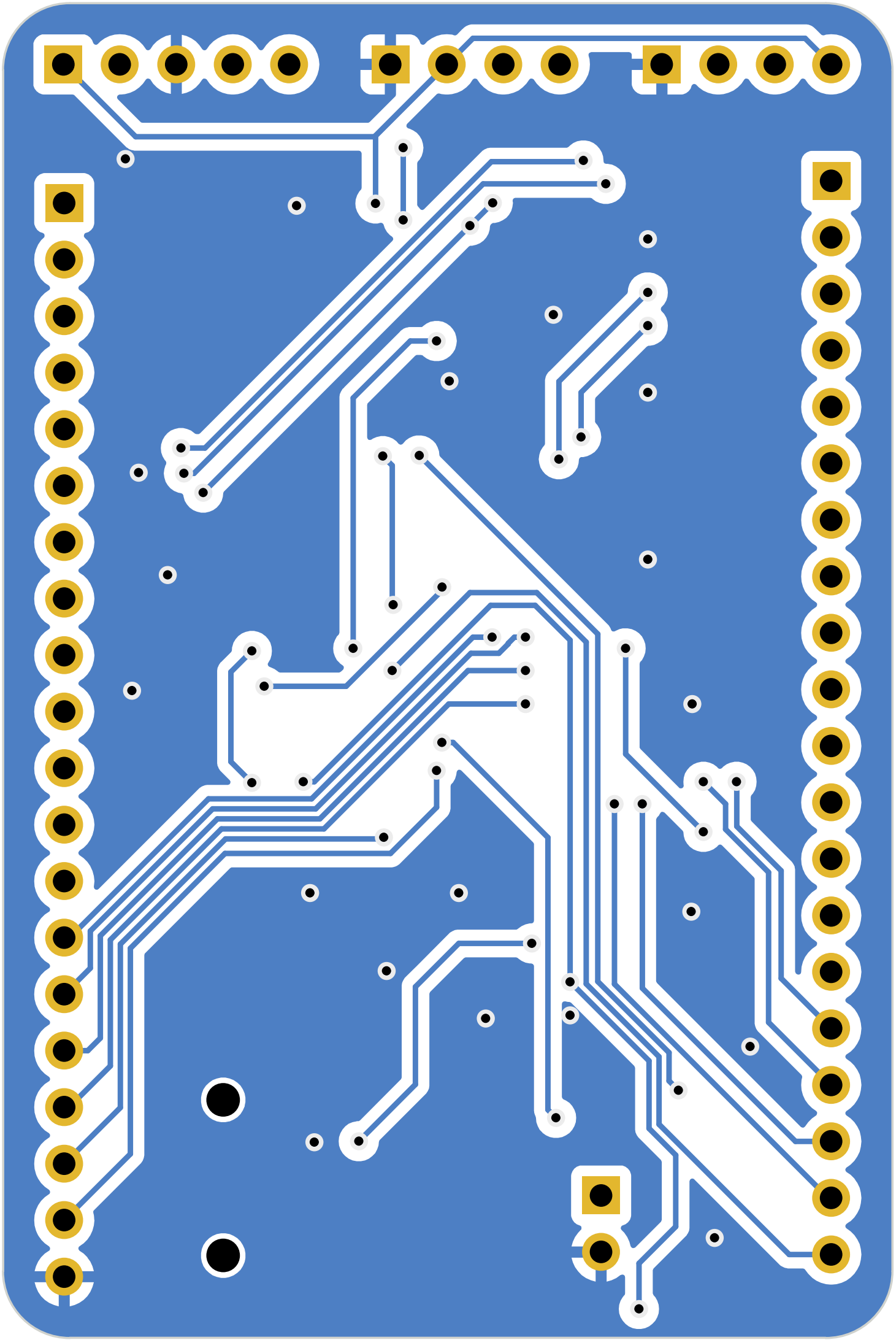
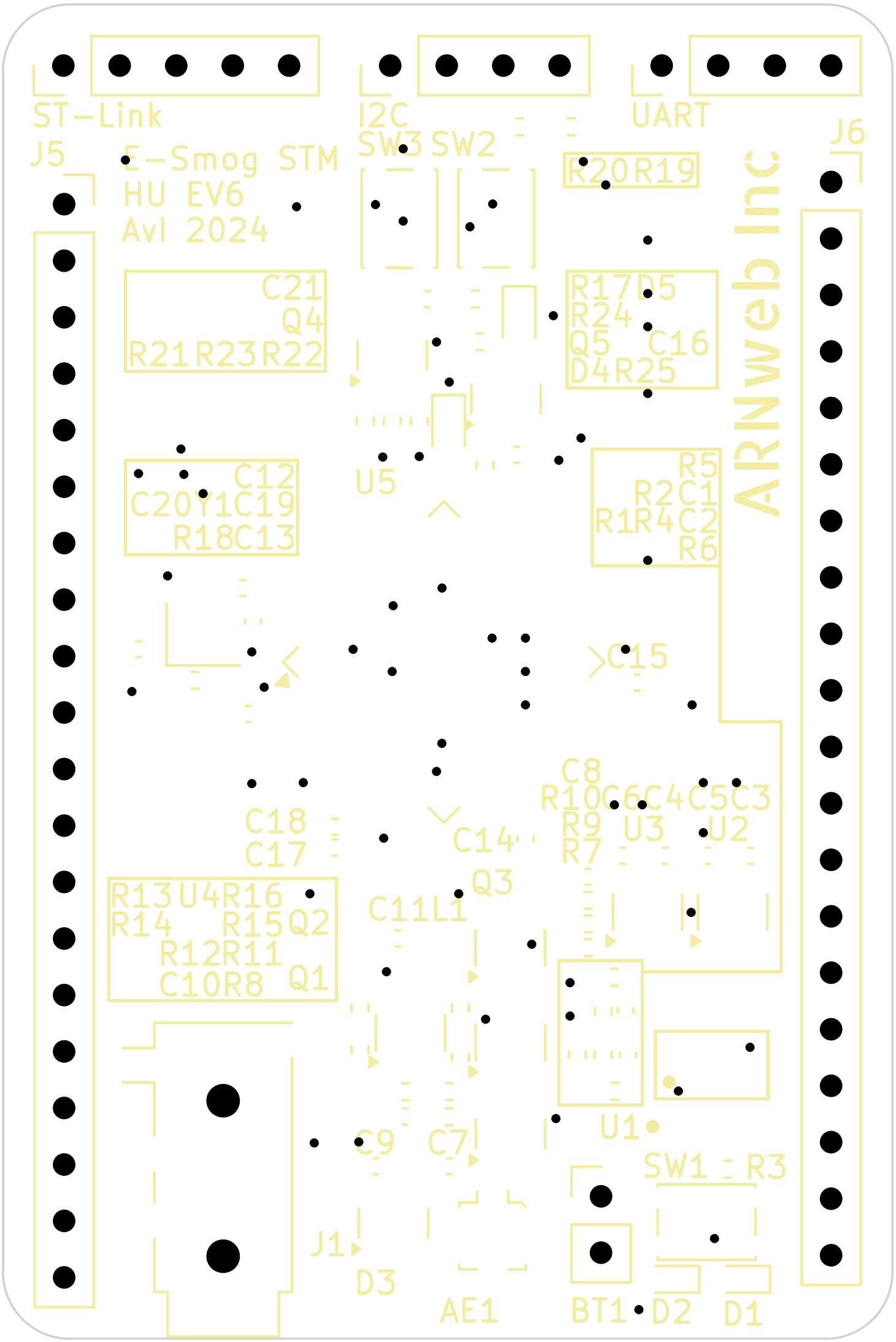
Q2
R12
R11
C10
R8
Q1
C11
L1
U1
C9
C7
SW1
R3
J1
D3
AE1
BT1
D2
D1






ST-Link
I2C
UART
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E-Smog STM
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Avl 2024
SW3
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C21
Q4
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ARNweb Inc
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C13
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C2
R6
C15
C8
R10
C6
C4
C5
C3
C18
C17
C14
R9
U3
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C11
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40 mm
60 mm